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PATENT
0033-0694P

IN THE U.S. PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF	BEFORE THE BOARD OF APPEALS
Masato SUMIKAWA et al.	Appeal No.:
APPL. NO.: 09/782,180	GROUP: 2814
FILED: February 14, 2001	EXAMINER: DiLinh Nguyen
CONF.: 3275	
FOR: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	

APPEAL BRIEF ON BEHALF OF APPELLANTS: TAKAYUKI NAKANO ET AL.

Assistant Commissioner for Patents
Washington, D.C. 20231

May 15, 2003

Sir:

This is the Appellants brief in response to a Final Rejection mailed September 19, 2002. A Notice of Appeal was filed March 19, 2003.

I. REAL PARTY IN INTEREST

The real party in interest for this application is the Assignee, Sharp Kabushiki Kaisha, of 22-22, Nagaike-cho, Abeno-ku, Osaka-shi, Osaka, Japan.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences regarding the subject matter of the present invention.

III. STATUS OF CLAIMS

Claims 1-17 are pending. Claims 1 is an independent claim from which claims 2-4 depend directly or through intervening claims.

Claim 5 is an independent claim from which claims 6-16 depend either directly or through intervening claims.

Claims 17 and 18 are independent claims.

IV. STATUS OF AMENDMENTS

1. A Reply After Final was submitted on December 19, 2002. This Reply was limited to a Request for Reconsideration. That Reply was considered as indicated in an Advisory Action mailed January 23, 2003.

2. A second Reply After Final was submitted on February 19, 2003. That Reply was limited to a Request for Reconsideration. To date, no Advisory Action has been received.

V. SUMMARY OF THE INVENTION

The present invention is directed to a semiconductor device and a method for making that device that can be packaged with enhanced resistance to breaking.

In the prior art, for example, as shown Figures in 5A and 5B of the present disclosure, the semiconductor can bend when it receives an external force caused, for example, when the device in which the semiconductor is included is dropped or receives an external force. The dropping or applying an external force, for example, causes a connection with the printed circuit board to break thus disconnecting the semiconductor device. See for example, a description of the background art on pages 1 and 2 of the present specification.

The present device and method have been provided for solving the problems of the prior art as set forth in the present specification. Basically, the structure of the semiconductor device is thin and has a mirror surface produced by abrasing and thereafter a reinforcing resin (see Fig. 1E, element 5) is provided. This resin reinforces the back surface of the semiconductor device. Thus, the semiconductor device has a reduced thickness so that it can bend while a level of rigidity can be assured as the semiconductor is reinforced with a back surface reinforcing member of resin.

In the method as shown in Figs. 1A to 1B, the surface of a semiconductor device opposite to the circuit side 2 is ground and then it is abrased by element 4 and is abrased to a mirror-finish. There is a protective tape 3 but this is removed as shown in Fig. 1B. After the grinding and abrasing to a mirror-finish, a reinforcing element 5 for example, of resin is applied to the semiconductor device.

The description of the invention has been made to comply with the Patent Office rules in submitting briefs and is not to be considered limiting the claimed invention.

VI. ISSUES

(1) Whether claims 1 and 17 are unpatenable under 35 U.S.C. §103(a) over Toyosawa (U.S. Patent 6, 337,257).

(2) Whether claims 2 and 4 are unpatenable under 35 U.S.C. §103(a) over Toyosawa (U.S. Patent 6,337,257) in view of Ohuchi (U.S. Patent 6,271,588).

(3) Whether claim 3 is unpatenable under 35 U.S.C. §103(a) over Toyosawa (U.S. Patent 6,337,257) in view of Ohuchi (U.S. Patent 6,271,588) and further in view of Horiuchi et al. (U.S. Patent 6,242,799).

(4) Whether claims 5-8 and 18 are unpatenable under 35 U.S.C. §103(a) over Tamaki et al. (U.S. Patent 6,136,688).

(5) Whether claims 9-12 are unpatenable under 35 U.S.C. §103 over Tamaki et al. (U.S. Patent 6,136,688) in view of Sakaguchi et al. (U.S. Patent 6,150,194).

(6) Whether claims 13-16 are rejected under 35 U.S.C. §103(a) as being unpatenable over Tamaki et al. (U.S. Patent 6,136,688) in view of Takahashi et al. (U.S. Patent 6,153,448).

The six rejections identified above are found in the Final Office Action of September 19, 2002.

VII. DESCRIPTION OF THE REFERENCES APPLIED

The references set forth below are listed in the sequence of the patent numbers.

(1) Tamaki et al. (U.S. Patent 6,136,668 issued October 24, 2000, Filing Date October 9, 1998).

In the portion relied on by the Examiner, the Examiner in explaining this reference relied on Fig. 7-10, column 7, lines 1-6. It is correct that a surface is ground and polished. Element 31 is an adhesive member as shown in Fig. 9, but this is not on the back surface of the semiconductor but is on the surface containing the functional element 7.

This reference does further disclose a metal reinforcement member element 9. This element as shown in Fig. 13 is on the surface of elements 5 and 7. Also, there is a second metal layer 11 and this is referred to in column 4 of the reference.

(2) Seguichi et al. (U.S. Patent 6,150,194 issued November 21, 2000, filed December 4, 1997).

In the rejection this patent was relied on show silicon resin can be printed for example by a screen printing. See column 4, lines 60-64.

(3) Takahashi (U.S. Patent 6,153,448 issued November 28, 2000, filed August 20, 1999).

This reference was applied by the Examiner to show spin coating of resin. See column 8, lines 52-50.

(4) Shigetsugu et al. (U.S. Patent 6,242,799 issued June 5, 2001, filed November 17, 1998).

This patent was cited to show a particular resin as set forth in column 5, lines 50-55.

(5) Ohuchi (U.S. Patent 6,271,588 issued on August 7, 2001, filed February 4, 2000).

This patent shows a protective tape 22 on a back surface of the semiconductor device. This tape is for protecting the semiconductor device so that dust inside a dye does not come in contact with a rear surface of the wafer. See column 3, lines 23-30. In a further processing of this device, the tape 22 is removed and the back surface is polished. See column 3, lines 66-column 4, line 5. The protective tape of this reference is a resin.

(6) Toyosawa (U.S. Patent 6,337,257 issued January 8, 2002, filed February 7, 2000).

This patent discloses, for example, a method of forming a semiconductor device wherein the back surface is ground and an etching is applied. See for example, column 5, line 66 - column 6, line 7. It is the position in the rejection that as this patent discloses a protective tape (not shown) during manufacture of the device the protective tape being on the second surface 36 of the chip. See column 12, lines 19-31. The assertion in the rejection that the not shown protecting tape is reinforcing element.

VIII. GROUPING OF CLAIMS

The grouping of claims will be as follows:

Claim 1 is separately grouped and stands or falls alone.

Claim 2 is separately grouped and stands or falls alone.

Claim 3 is separately grouped and stands or falls alone.

Claim 4 is separately grouped and stands or falls alone.

Claim 5 and its depending claims 6-8 are separately grouped and stand or fall together.

Claims 9-12 are grouped together and stand or fall together.

Claims 13-16 are grouped together and stand or fall together.

Claim 17 has been separately grouped and stands or falls alone.

Claim 18 has been separately grouped and stands or falls alone.

The separately grouped claims are separately argued in accordance with USPTO rules and *In re Beaver* 13 USPQ 2d 1409 (Fed. Circuit 1989).

IX. ARGUMENTS

In the first instance, the final rejection of all the claims does not establish a *prima facie* case of obviousness. A *prima facie* case of obviousness is the burden under 35 U.S.C. §103 of the USPTO as set forth in *In re Fine* 837F 2nd 1071, 5 USPQ 2nd 1596 (Fed. Circuit 1998).

The *prima facie* case of obviousness has not been established for any one of the reasons as follows:

(1) Outside of the Applicants own disclosure and teachings, there is no suggestion (motivation) to combine the art to arrive at the subject matter claimed; or

(2) The combination of references does not suggest the steps or structure specifically claimed.

ARGUMENT DIRECTED TO THE REJECTION OF CLAIMS 1 AND 17 AS BEING UNPATENABLE OVER TOYASAWA (U.S. PATENT 6,337,257)

The basic reason for the rejection of these claims is that the protective tape on the back surface of the semiconductor chip has a protective tape (not shown) and this protective tape as asserted inherently provides reinforcement. See column 12, lines 28-31.

Initially, claim 1 requires that the back surface has a physical structure of being abrased so it has a mirror [reflective] finish and reinforced with a back surface reinforcing member. While the back surface 36 of the reference can be ground and polished to a mirror smooth surface by etching this does not suggest the physical structure of abrased of the back surface. More importantly, the back surface reinforcing member is not found either specifically or inherently in the reference. It has been apparently the position of the Examiner that the protective tape inherently provides a reinforcement. See the comments in the Advisory Action mailed January 23, 2003. Also the protective tape is used only in a manufacturing step and does not form structure of the chip in the context claimed.

Furthermore, in an interview, the primary Examiner stated that because semiconductor films are "thin" inherently the protective tape of the reference would reinforce. This comment was traversed. See a letter regarding the interview dated February 27, 2003, which is attached as attachment "A".

Initially in the art, the term reinforcement and protective when applied to semiconductors has two distinct meanings. See for example, the present specification and some of the references cited below in which this matter will be further explained. Also the results of using the reinforcement in the article is to allow bending but still protect the connection of the electrical connections claimed.

Also while it was asserted that semiconductor chips are "thin" this is a relative term. In fact, in column 12 of U.S. Patent 6,337,257, the semiconductor chips have a high

mechanical strength. See column 12, lines 32-38. Also, in the disclosure of this patent, the semiconductor chip can be for example 400 μm also the reference shows that the protective tape can be as small as 130 μm. See column 12, line 47. Certainly, a tape which is protective and is substantially thinner than the semiconductor chip it is submitted could not mechanically be a reinforcement.

It appears in rejecting the claim inherency which is generally applicable to a rejection under 35 U.S.C. §102 was relied on. See the comments to the interview. At best even if the protective tape is a reinforcement, (which it is not as explained above) a rejection on inherency cannot be based on possibility or probability. See Continental Can Co. USA. v. Monsanto Co. 20 USPQ 2nd 1749 (Fed. Circuit) 1991 wherein the court stated as follows:

> Inherency...may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a different set of circumstances is not sufficient...

While this case dealt with a rejection under 35 U.S.C. §102, because of the rejection of claim 1 the doctrine set forth appears to be applicable here. This comment is made because it is understood that in rare instances, a rejection under 35 U.S.C. §103 is the epitome of a rejection under 35 U.S.C. §102.

Of course if a rejection is specifically made under 35 U.S.C. §102, the Applicants request that they be given an opportunity to respond as this would be a new rejection.

Claim 17 which is an article is somewhat broader than claim 1. This claim does distinguish over the reference because there is no "back surface reinforcing member on said second surface" the arguments regarding this difference have been addressed in the reply to the rejection of claim 1 is *supra* and which is incorporated herein. For example, even if the protective tape of the base reference was resin, it is not a reinforcement member.

ARGUMENTS AS TO THE REJECTION OF CLAIMS 2 AND 4 UNDER 35 U.S.C. §103 BASED ON TOYOSAWA , OHUCHI AND HORIUCHI

Claim 4 includes specific resins. While these resins may be known, in the combination the specific resins provide a result not shown or expected in the art. See the paragraph bridging pages 2 and 3 of the specification which states as follows:

> In the present invention still preferably the resin is formed of a material having an elastic modulus of 1.5 x 10^6 N/m^2 to 5.0 x 10^6 N/m^2. More specifically, the resin is selected from the group consisting of resin of rubber type, resin of silicone type, resin of epoxy type, resin of polymide type and resin of urethane type. Thus the resin can reinforce the semiconductor substrate without impairing the bendability of the substrate. Applying such resins can also prevent the substrate from chipping or being scratched.

With respect to claim 2 there is no suggestion to use resin for the not shown tape of the base reference.

It appears that the rejection has given no consideration to the results achieved. Results that are not expected are evidence of non-obviousness and must be considered in a rejection under 35 U.S.C. §103.

ARGUMENT AS TO THE REJECTION OF CLAIM 3 UNDER 35 U.S.C. §103 BASED ON TOYOSAWA, OHUCHI AND HORIUCHI

Claim 3 is dependent on claim 2. It was the position of the Examiner that the specific resin was known. Even if this resin was known, the resin specifically claimed in the combination provides a specific result which again has not been taken into consideration in the rejection as explained *supra*. Also, the Examiner relies on Ohuchi and asserts that this reference also shows what is substantially claimed. But a fair reading of this reference does indicate that element 22 is a protective tape to protect the semiconductor chip while it is in a dye. In the final article, the protective tape 22 is not a reinforcement tape as explained in the rejection based on the first reference. Also, the protective tape is peeled and then the

surface is polished. Of course this is related to the method. But in summary, while the protective tape of Ohuchi is resin, it does not cure the inherent deficiencies of the rejection based on the first reference.

Also the specific resin claimed is important. See the paragraph bridging pages 8 and 9 of the specification.

ARGUMENTS RELATIVE TO THE REJECTION OF CLAIMS 5-8 AND 18 UNDER 35 U.S.C. §103 AS BEING UNPATENABLE OVER TAMAKI.

Claim 5 is a method claim. In rejecting this claim, the Examiner asserted that element 31 as described in Figs. 7-10 and column 7, lines 1-6 of Tamaki was the reinforcement member claimed. But element 31 is an adhesive which during manufacture holds a reinforcing plate 21. This reinforcing plate of course is detached and is not applied to the back surface of element 1. The semiconductor chip is shown in Figs. 9 and 10.

As explained in the summary of this reference, Tamaki does disclose a reinforcing member 9, but this reinforcing member is not on the back surface but is on metal layers 5 and 7. See for example, column 10, Fig. 24. But even considering the totality of the reference, claim 5 distinguishes over the reference because claim 5 abrases to a mirror finish. This is not shown or suggested in the totality of the reference. Also the resin is applied to the surface abrased which is opposite to a surface having an external connection electrode. In the reference, the reinforcement member is metal. Furthermore, there is no electrical connection in the context claimed. While the reference does show element 3 on the top surface of the semiconductor device this is not an electrode connection and is only disclosed as a "functional device".

Accordingly, there is no suggestion from this reference to arrive at the Applicants method claim set forth in claim 5.

With respect to claim 18, this claim is broader than claim 5. This claim does have the step of providing an external connection electrode on a second surface and applying resin on the mirror finish surface. As explained above, this is not shown or suggested by the reference applied. With respect to claims 6-8 these claims are grouped with claim 5.

ARGUMENT AS TO THE REJECTION OF CLAIMS 9-12 UNDER 35 U.S.C. §103 OVER TAMAKI IN VIEW OF SAKAGUCHI.

In the first instance, claim 9 is dependent on claim 5, claim 10 is dependent on claim 6, claim 11 is dependent on claim 7 and claim 12 is dependent on claim 8.

These claims in the first instance are considered patenable at least for the same reasons as their base or intervening claims. In applying the rejection to these claims, the Examiner has also relied on a reference to Sakaguchi et al. (U.S. Patent 6,150,194). The Examiner relied on column 4, lines 60-64 to show printing of a resin. But again the Examiner has not given significance to the result achieved.

In the specification it is specifically set forth that by applying the reinforcement resin by printing highly viscous resins can also be distributed and thus applied. See page 3, lines 19-21 of the specification. Accordingly, again the Examiner has not given any significance to the result achieved. Preferably, resin 5 is of material having a small elastic modulus of approximately 1.5 to 5.0 x 10^6 N/m^2 since resin 5 with such a small elastic modulus does not impair the bendability of LSI chip 7. Such a value of elastic modulus is small relative to that of LSI chip 7 and it is thus a negligible value for the entirety of a package, and applying resin 5 on LSI chip 7 can prevent the chip from chipping or being scratched, which allows the chip to be handled more readily. Resin 5 is applied in an amount that can be set as desired in a range that does not affect on the bendability of the entire package. Desirably, resin 5 is reduced in thickness in a range that can prevent LSI chip 7 from chipping or being

scratched, to approximately several tens μm as the package can be decreased in thickness and its material cost can also be reduced.

ARGUMENT AS TO THE REJECTION OF CLAIMS 13-16 UNDER 35 U.S.C. §103 BASED ON TAMAKI IN VIEW OF TAKAHASHI.

In rejecting these claims, the Examiner has used the additional reference to Takahashi et al., which does disclose in column 8, lines 51-54 (a spun resin layer). This resin layer is for sealing and is not on the surface of the semiconductor layer as defined in the base claim 5. Furthermore, it again appears that the Examiner has not given any significance to the results achieved therein. That is, by applying the resin, which is a reinforcement resin by spin coating, the resin can be applied rapidly reduced in thickness uniformly as explained in the specification page 3, lines 22-24.

SUMMARY OF ARGUMENTS

For the reasons explained above, there is no *prima facie* case of obviousness established. Also, it appears that the Examiner has given no significance to the results achieved in the article and method. An analysis of obviousness of a claim combination must include consideration of the results achieved by the combination. See The Gillette Co. U.S.C. v. Johnson & Sons, Inc. 16 USPQ 1923, 1928 (Fed Circuit 1990) wherein the court stated as follows:

> An analysis of obviousness of a claimed combination must include consideration of the results achieved by that combination, as we explained in *Interconnect Planning Corp. v. Feil*, 774,F.2d 1132, 1143, 227 USPQ 543, 551 (Fed. Cir. 1985).

Also it appears in making the rejection under 35 U.S.C. §103, the Examiner has concentrated not on the subject matter as a whole as required in 35 U.S.C. §103 but on the substitution of the parts or steps. This is improper in making a rejection under 35 U.S.C. §

103. See Hybritech Inc. v. Monoclonial Antibodies, Inc. 231 USPQ 81 (Fed. Circuit 1986) (also cited in MPEP) wherein the court stated as follows:

> Focusing on the obviousness of substitutions and the differences instead of on the invention as a whole...was a legally improper way to simplify the difficult determination of obviousness.

Additionally it is recognized that in examination the USPTO can give a reasonable interpretation of words in the claims under MPEP 2111. To call a protective tape a reinforcing member is not reasonable and is a "play on words" as the present disclosure makes this distinction. Also patent 6,271,588 refers to a protective tape 22 while 6,136,668 refers to reinforcement layer 9. This is evidence that one skilled in the art recognizes the different structure and function and the Examiners assertion that these elements (protection and reinforcement) are the same is repugnant to these terms as one skilled in the art would understand. Thus, the Examiner's assertion is not reasonable. Also see MPEP 2111 last paragraph which discusses this point.

X. CONCLUSION

For the reasons specifically set forth above, the outstanding rejections set forth in the Final Office Action be reversed.

Respectfully submitted,
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APPENDIX OF CLAIMS

1. A semiconductor device comprising:

a semiconductor substrate having a surface provided with an external connection electrode and;

a surface opposite that with said external connection electrode, abrased with a mirror finish and reinforced with a back-surface reinforcement member.

2. The semiconductor device of claim 1, wherein said back-surface reinforcement member is formed of resin.

3. The semiconductor device of claim 2, wherein said resin is formed of a material having an elastic modulus of 1.5×10^6 N/m^2 to 5.0×10^6 N/m^2.

4. The semiconductor device of claim 2, wherein said resin is selected from the group consisting of resin of rubber type, resin of silicone type, resin of epoxy type, resin of polyimide type and resin of urethane type.

5. A method of manufacturing a semiconductor device comprising the steps of:

abrasing to a mirror finish a surface of a semiconductor substrate opposite to a surface thereof having an external connection electrode; and

applying resin on said surface abrased.

6. The method of claim 5, further comprising the step of cutting said semiconductor substrate after the step of applying.

7. The method of claim 5, further comprising the step of previously grinding said surface to be abrased.

8. The method of claim 6, further comprising the step of previously grinding said surface to be abrased.

9. The method of claim 5, wherein in the step of applying, said resin is printed.

10. The method of claim 6, wherein in the step of applying, said resin is printed.

11. The method of claim 7, wherein in the step of applying, said resin is printed.

12. The method of claim 8, wherein in the step of applying, said resin is printed.

13. The method of claim 5, wherein in the step of applying, said resin is applied by spin-coating.

14. The method of claim 6, wherein in the step of applying, said resin is applied by spin-coating.

15. The method of claim 7, wherein in the step of applying, said resin is applied by spin-coating.

16. The method of claim 8, wherein in the step of applying, said resin is applied by spin-coating.

17. A semiconductor device comprising:

a semiconductor substrate having a first surface with an external connection electrode;

a second surface which is a mirror finished surface opposite to said first surface; and

a back surface reinforcement member on said second surface which is mirror finished.

18. A method of manufacturing a semiconductor device comprising the steps of:

providing a mirror finished surface on a first surface of a semiconductor substrate;

providing an external connection electrode on a second surface which is opposite to the first surface; and

applying resin on the mirror finished surface.

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APPEAL BRIEF

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